THE OPEN UNIVERSITY OF SRI LANKA

DEPARTMENT OF MATHEMATICS AND COMPUTER SCIENCE

B. SC. DEGREE PROGRAMME 2013/2014

FINAL EXAMINATION

CPU3141: DIGITAL COMPUTER FUNDAMENTALS

DURATION: TWO HOURS (2 HOURS)

Date: 12.11.2014 **Time: 1.30 pm – 3.30 pm**

Answer **FOUR** Questions **ONLY.**

Q1.

(i) What is the number system used in digital computers? Give two reasons why the particular system is used in computers?

(ii) Convert the following **decimal numbers** into **binary.**

a) 57_{10}

b) 137.25_{10}

c) -45_{10}

d) -6.625_{10}

(iii)

a) What is **BCD**?

b) What are the differences in **Gray Code** and **BCD** and their different applications? (give 02)

(iv) Convert the following words into ASCII code (ASCII Table is in Appendix). Present your answer in base 16.

DIGITAL COMPUTER

Butterfly

Q2.

(i) What are the results of the following operations when **A = 1** and **B = 1.** Briefly justify your answer in words.

- A + B when A and B are Boolean.
- A + B when A and B are binary.

(ii)

a. Use the following truth table to derive **POS** term for the output X

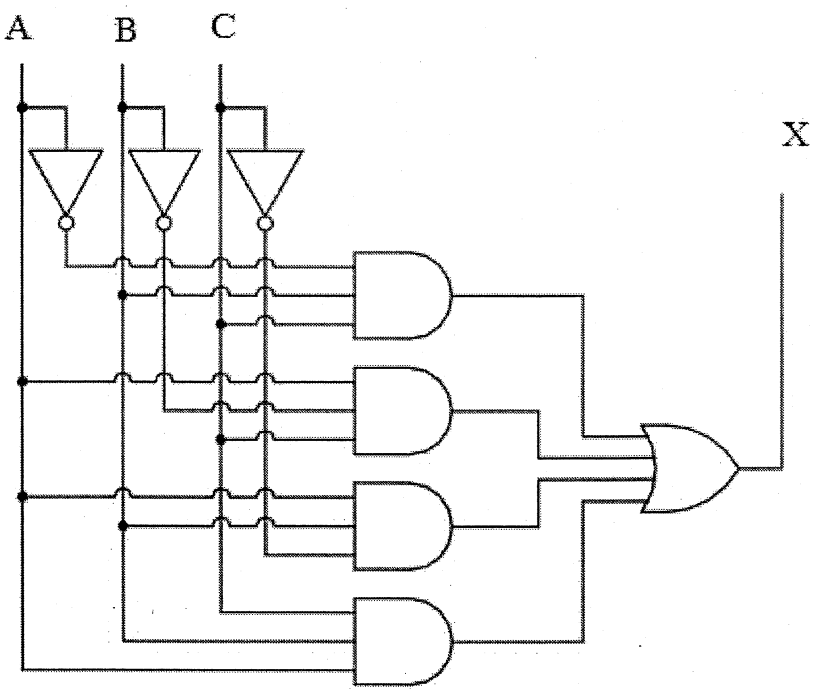
b. Simplify the above POS term using **K-Map** (Karnaugh Map) method.

A	B	C	D	X
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

(iii) Consider the following **Logic Circuit.**

a. Simplify the circuit using **Boolean Algebraic Rules.**

b. Draw the simplified circuit diagram using appropriate logic gates.



Q3.

(i)

a. Draw the truth table and the logic circuit for a Half Adder.

b. Draw the logic circuit above (part a) for Half Adder using XOR gates.

(ii) Decoder is a circuit that changes a code into a set of signals.

a. Draw the truth table for a **2-to-4 Decoder**.

b. Draw the logic circuit for the **2-to-4 Decoder**.

c. Draw the block diagram design of a **2-to-4 Decoder** using only **1-to-2 Decoders**.

(iii)Explain the operation of a **DeMultiplexer** using a block diagram. List two (**02**) uses of **Demultiplexers**.

Q4.

(i)

a. What is a **Sequential Logic Circuit**?

b. What are the classes of Sequential Circuits?

(ii) Describe the function of the **Master-Slave JK flip-flop**. (Use block **diagrams.**)

(iii)Describe the function of a **Shift Register** using a block diagram of any one of the four types of Shift Registers?

(iv) Draw the **timing diagram** for the **four bit synchronous counter**.

Q5.

(i) List five (05) properties of **Asynchronous Sequential Circuits.**

(ii) What is **Race Condition**? Explain with examples.

(iii) Draw the **block diagram** and **truth table** for a **asynchronous decade counter**.

(iv) Discuss **four(04) advantages** of **asynchronous counters**.

Q6.

(i) What are the steps the **Central Processing Unit** perform for each instruction once the necessary data and instruction are in memory?

(ii) How does data and instructions are transferred from an input device into the memory?

(iii) ***Reads*** dominate processor cache accesses. All instruction accesses are *Reads*. What are the ***Read*** **policies**, and briefly describe them.

(iv)Describe how the **CPU (Central Processing Unit)**, in association with the **memory,** executes a computer program.

***** End of Paper*****

Appendix - ASCII Table

Dec	Hex	Name	Char	Ctrl-char	Dec	Hex	Char	Dec	Hex	Char	Dec	Hex	Char
0	0	Null	NUL	CTRL-@	32	20	Space	64	40	@	96	60	`
1	1	Start of heading	SOH	CTRL-A	33	21	!	65	41	A	97	61	a
2	2	Start of text	STX	CTRL-B	34	22	"	66	42	B	98	62	b
3	3	End of text	ETX	CTRL-C	35	23	#	67	43	C	99	63	c
4	4	End of xmit	EOT	CTRL-D	36	24	$	68	44	D	100	64	d
5	5	Enquiry	ENQ	CTRL-E	37	25	%	69	45	E	101	65	e
6	6	Acknowledge	ACK	CTRL-F	38	26	&	70	46	F	102	66	f
7	7	Bell	BEL	CTRL-G	39	27	'	71	47	G	103	67	g
8	8	Backspace	BS	CTRL-H	40	28	(	72	48	H	104	68	h
9	9	Horizontal tab	HT	CTRL-I	41	29	)	73	49	I	105	69	i
10	0A	Line feed	LF	CTRL-J	42	2A	*	74	4A	J	106	6A	j
11	0B	Vertical tab	VT	CTRL-K	43	2B	+	75	4B	K	107	6B	k
12	0C	Form feed	FF	CTRL-L	44	2C	,	76	4C	L	108	6C	l
13	0D	Carriage feed	CR	CTRL-M	45	2D	-	77	4D	M	109	6D	m
14	0E	Shift out	SO	CTRL-N	46	2E	.	78	4E	N	110	6E	n
15	0F	Shift in	SI	CTRL-O	47	2F	/	79	4F	O	111	6F	o
16	10	Data line escape	DLE	CTRL-P	48	30	0	80	50	P	112	70	p
17	11	Device control 1	DC1	CTRL-Q	49	31	1	81	51	Q	113	71	q
18	12	Device control 2	DC2	CTRL-R	50	32	2	82	52	R	114	72	r
19	13	Device control 3	DC3	CTRL-S	51	33	3	83	53	S	115	73	s
20	14	Device control 4	DC4	CTRL-T	52	34	4	84	54	T	116	74	t
21	15	Neg acknowledge	NAK	CTRL-U	53	35	5	85	55	U	117	75	u
22	16	Synchronous idle	SYN	CTRL-V	54	36	6	86	56	V	118	76	v
23	17	End of xmit block	ETB	CTRL-W	55	37	7	87	57	W	119	77	w
24	18	Cancel	CAN	CTRL-X	56	38	8	88	58	X	120	78	x
25	19	End of medium	EM	CTRL-Y	57	39	9	89	59	Y	121	79	y
26	1A	Substitute	SUB	CTRL-Z	58	3A	:	90	5A	Z	122	7A	z
27	1B	Escape	ESC	CTRL-[	59	3B	;	91	5B	[	123	7B	{
28	1C	File separator	FS	CTRL-\	60	3C	<	92	5C	\	124	7C	|
29	1D	Group separator	GS	CTRL-]	61	3D	=	93	5D	]	125	7D	}
30	1E	Record separator	RS	CTRL-^	62	3E	>	94	5E	^	126	7E	~
31	1F	Unit separator	US	CTRL-_	63	3F	?	95	5F	_	127	7F	DEL